APPLICATION NOTE **DATE: 4/1/96**

EPROM Security on the H8/300, H8/300L, H8/500, H8/300H and SH7000 families

The H8/300 (L), H8/300H, H8/500 and SH7000 microcontrollers have an EPROM security feature that can be used by the application programmer. This feature allows the user of the microcontroller to protect parts (or all) of the code programmed into the on chip EPROM of the device from being read by means other than his or her own program. Due to the nature of this feature it cannot be tested by Hitachi and is therefore not guaranteed . It is up to the user to determine whether or not to implement the features of this function and accept sole responsibility for its outcome.

Memory Configuration:

The memory matrix of the H8 and SH microcontroller is configured as a dual matrix, one with even addresses and one with odd addresses. The configuration of each matrix appears as lines of memory 32 bytes wide (32 x 8, 256 bits). This configuration allows an individual memory line to consist of 64 bytes data (including both even and odd addressing). Each memory line has 1 security bit thus allowing every 64 byte segment to have the option of the security feature. The address of this security bit is the same as the starting address for the memory line.

Security Functions:

The security function has two different operations depending on the mode of operation that the device is placed into; EPROM programming mode or CPU operation mode.

EPROM Programming mode:

In the EPROM programming mode, the ability of the EPROM programmer to read the EPROM contents is limited by the state of the security bit.
If the security bit is a ‘1’ (unprogrammed state), then the data in the EPROM can always be read. If the security bit is a ‘0’ (programmed state), then any read operation to the EPROM will result in a ‘00’ being read. This indicates that once the security bit is programmed, the user will be unable to verify the contents of the EPROM.

security bit 1	EPROM can be read (normal)
security bit 0	“00” data can be read.

CPU operating mode:

In the CPU operating mode, the ability of any device to read the EPROM contents is limited by the state of the security bit.
If the security bit is a '1' (unprogrammed state), then the data in the EPROM can always be read. If the security bit is a '0' (programmed state), then the read state of the EPROM (from the CPU) depends upon where the instruction execution is occurring from.

security bit 1 EPROM data can be read (normal)
security bit 0 After reset, the CPU can read EPROM data until it executes an instruction outside the internal EPROM area (either external memory or internal RAM). Once an instruction is executed outside the internal EPROM memory area, then the EPROM becomes disabled and cannot be accessed any further. This prohibits an external program from being able to "dump" the contents of the internal on-chip EPROM.

Programming the Security bit:

There exist two EPROM programming modes; Normal and Security. The Normal programming mode allows the user to program the code/data area of the on-chip memory of the device. The Security programming mode allows the user to program the security bits, thus implementing the security feature. The security function is implemented by programming a '0' into the address corresponding to the memory line location. Setting the programming mode is accomplished by setting certain I/O port/Address Line pins as shown in the Following table.

H8/300 Family Programming modes

Device	Programming Mode	Port Pins
H8/325 Family	Normal	$P7_0$=1 $P7_1$=1
	Security	$P7_0$=1 $P7_1$=0
H8/330	Normal	$P8_0$=1 $P8_1$=1
	Security	$P8_0$=1 $P8_1$=0
H8/338 Family	Normal	$P6_4$=1 $P6_3$=1
	Security	$P6_4$=1 $P6_3$=0
H8/350	Normal	$P8_0$=1 $P8_1$=1
	Security	$P8_0$=1 $P8_1$=0

H8/300L Family Programming modes

Device	Programming Mode	Port Pins
H8/3834 Family	Normal	$P1_1$=1 $P1_2$=1
	Security	$P1_1$=1 $P1_2$=0
H8/3837 Family	Normal	$P1_1$=1 $P1_2$=1
	Security	$P1_1$=1 $P1_2$=0
H8/3614 Family	Normal	$P4_2$=1 $P4_3$=1
	Security	$P4_2$=1 $P4_3$=0

H8/500 Family Programming modes

Device	Programming Mode	Port Pins
H8/520	Normal	$P5_0$=1 $P5_1$=1
	Security	$P5_0$=1 $P5_1$=0
H8/532	Normal	$P6_0$=1 $P6_1$=1
	Security	$P6_0$=1 $P6_1$=0
H8/534	Normal	$P6_0$=1 $P6_1$=1
	Security	$P6_0$=1 $P6_1$=0
H8/536	Normal	$P6_0$=1 $P6_1$=1
	Security	$P6_0$=1 $P6_1$=0

H8/300H Family Programming modes

Device	Programming Mode	Port Pins
H8/3032	Normal	$P5_0$=1 $P5_1$=1
	Security	$P5_0$=1 $P5_1$=0
H8/3042	Normal	$P5_0$=1 $P5_1$=1
	Security	$P5_0$=1 $P5_1$=0
H8/3047	Normal	$P5_0$=1 $P5_1$=1
	Security	$P5_0$=1 $P5_1$=0
H8/3048	Normal	$P5_0$=1 $P5_1$=1
	Security	$P5_0$=1 $P5_1$=0

SH7000 Programming modes

Device	Programming Mode	Port Pins
SH7034	Normal	A17=1 A18=1
	Security	A17=1 A18=0

Again, this feature cannot be tested by Hitachi and therefore cannot be guaranteed. It is up to the user to determine whether or not to implement the function of this feature and accept sole responsibility for its outcome