Application Notes

Hitachi Single-Chip Microcomputer

Technical Questions and Answers

H8/500 CPU

How to Use Microcomputer Technical Questions and Answers

Technical Questions and Answers has been created by arranging technical questions actually asked by users of Hitachi microcomputers in a question-and-answer format. It should be read for technical reference in conjunction with the User’s Manual.

Technical Questions and Answers can be read before beginning a microcomputer application design project to gain a more thorough understanding of the microcomputer, or during the design process to check up on difficult points.

Contents

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 001B
Topic	Register contents after power-up reset		

Question

1. What are the CPU register contents after a power-up reset?

Answer

1. In minimum mode, the program counter is loaded from the vector table. The interrupt mask bits (I_2, I_1, I_0) in the status register (SR) are set to 1, and the trace bit (T) is cleared to 0. Registers R0 to R7, the base register (BR), and the other SR bits have undetermined values.

   In maximum mode the code page register (CP) is loaded from the vector table. Other page registers have undetermined values. Registers other than the page registers are the same as in minimum mode.

Classification—H8/500

❍	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 002B
Topic	Page registers in single-chip mode and expanded minimum modes		

Question

1. Can the DP, EP, and TP page registers be used as data registers in the single-chip mode and expanded minimum modes?

Classification—H8/500

❍	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. Yes, but since the page registers are control registers, they can only be accessed by system control instructions (LDC, STC).

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 036A
Topic	DP contents in unconditional jump within page		

Question

1. If the JMP @R0 unconditional in-page jump instruction is executed in expanded maximum mode, are the data page (DP) register contents used in calculating the effective address?

Classification—H8/500

❍	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. The DP contents are not used in calculating the effective address of an unconditional jump within the same page.

   If the JMP @R0 instruction is executed to jump within the same page, the R0 contents are loaded into the program counter (PC), but the code page (CP) register value does not change. The DP contents are therefore ignored.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 004B
Topic	Interrupt sampling and acceptance		

Question

1. When are external interrupts (NMI, IRQ_n) sampled?

Classification—H8/500

	Registers
	Read timing
	Write timing
❍	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. Level-sensitive interrupts (IRQ_0) are sampled on the rising edge of the system clock. Edge-sensitive interrupts (external interrupts other than IRQ_0) are sampled on the falling edge of the system clock.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 006B
Topic	Holding of disabled external interrupts		

Question

1. In the following two cases, are external interrupts (IRQ_n) held pending?

   (1) IRQ_n enable bit is cleared to 0 in on-chip register field

   (2) IRQ_n interrupt priority level ≤ interrupt mask level set in status register (SR)

Classification—H8/500

	Registers
	Read timing
	Write timing
❍	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. (1) In this state, the interrupt request signal is not sampled and the interrupt is not held pending. Interrupt requests made in this state will be ignored even if the IRQ_n enable bit is later set to 1.

   (2) An interrupt that is requested in this state is held pending in the CPU's interrupt controller. If the interrupt request mask level is later reduced to a value lower than the external (IRQ_n) interrupt priority level, the interrupt will be accepted.

   IRQ_0 is level-sensitive, however, so it is not held pending.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

The interrupt request mask level is set in bits I_2 to I_0 in the status register (SR).

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 008A
Topic	Disabling of invalid instruction exceptions		

Question

1. Can exception handling of invalid instructions be disabled? How does the exception handling routine terminate?

Classification—H8/500

	Registers
	Read timing
	Write timing
❍	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. No, it cannot be disabled.

   The invalid instruction exception handler cannot be terminated by returning with an RTE instruction. Use some other software technique, such as jumping to the reset routine.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 028A – 1
Topic	Interrupt contention while waiting for instruction execution to end		

Question

1. Suppose an interrupt occurs during execution of an instruction, then during the waiting state before the instruction ends another, higher-priority interrupt occurs. Which interrupt does the CPU accept?

Classification—H8/500

	Registers
	Read timing
	Write timing
❍	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. The CPU accepts the interrupt with the highest priority level four states before the time of acceptance. (See the next page.) The interrupt mask level in bits I_2 to I_0 is not changed until the status register (SR) has been saved onto the stack.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

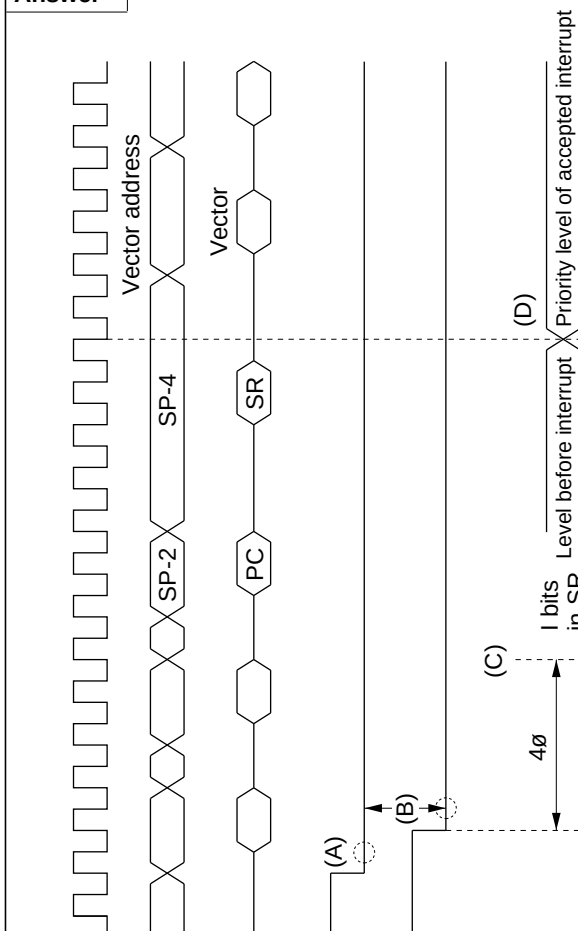
Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 028A – 2
Topic	Interrupt contention while waiting for instruction execution to end		

Answer



(A) Interrupt source 1 is input but not accepted because of instruction execution.

(B) Interrupt sources 1 and 2 contend. Interrupt source 2 is selected.

(C) The instruction being executed ends. The CPU accepts interrupt source 2.

(D) The I bits in the status register are changed to level 7.

Note: Conditions: minimum mode with the program and stack areas both in on-chip memory and interrupt handler starting at an even address.

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 030A – 1
Topic	Time of clearing of IRQ_n interrupt request signal		

Question

1. There are no interrupt request flags for edge-sensitive external interrupts (IRQ_n). When are these requests cleared?

Answer

1. The interrupt request is cleared during the internal cycle in which the interrupt is accepted, as indicated by the arrow in the diagram on the next page. If the same interrupt request signal (IRQ_n) occurs after this time, it will be latched again.

Classification—H8/500

	Registers
	Read timing
	Write timing
❍	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

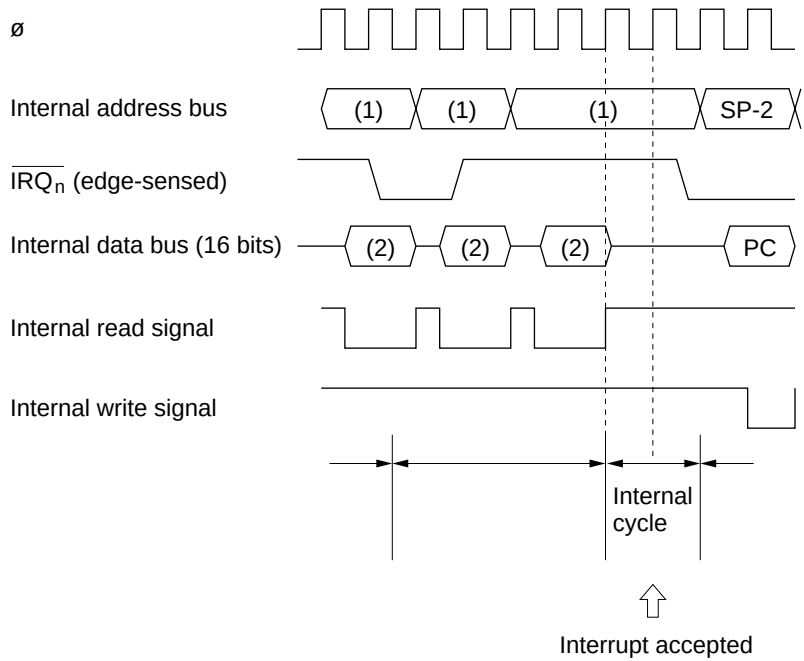
Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	**Q&A No.**	QA8500 - 030A – 2
Topic	Timing of clearing of IRQ_n interrupt request signal		
Answer			



(1) Instruction prefetch address (2) Instruction code

Taken from the User's Manual

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 031A
Topic	Requirements for enabling interrupts		

Question

1. Why do we fail to get an interrupt even though the interrupt request enable bit (IRQ_nE) is set to 1 and the interrupt request signal ($\overline{IRQ_n}$) is asserted?

	Classification—H8/500
	Registers
	Read timing
	Write timing
❍	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. To enable interrupts to be accepted, software must:

   (1) Set the interrupt enable bits for the desired interrupt sources to 1.

   (2) Set values in the interrupt priority registers (IPRs).

   (3) Set the desired interrupt request mask level in bits I_2 to I_0 in the status register (SR).

   Check the above points.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

A reset initializes all IPR values to 0 and sets bits I_2 to I_0 all to 1, masking all interrupts except NMI.

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 032A
Topic	Maximum wait after $\overline{\text{BREQ}}$		

Question

1. What is the maximum waiting time from input of an external bus request signal ($\overline{\text{BREQ}}$) until the CPU replies ($\overline{\text{BACK}}$)?

Answer

1. The maximum waiting time is 10 to 17 states. This occurs if the CPU started executing the MOVFPE or MOVTPE instruction (which transfers data in synchronization with the E clock) just before $\overline{\text{BREQ}}$ was asserted. Because MOVTPE and MOVFPE execute in synchronization with the E clock, the number of states varies depending on the timing of the start of execution.

Classification—H8/500

	Registers
	Read timing
	Write timing
❍	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 034A
Topic	Clearing of interrupt request enable bits and pending interrupts		

Question

1. While an IRQ_n interrupt is being held pending because its priority is equal to or less than the interrupt request mask level in the status register (SR), does clearing the IRQ_n enable bit (IRQ_nE) also clear the IRQ_n interrupt request?

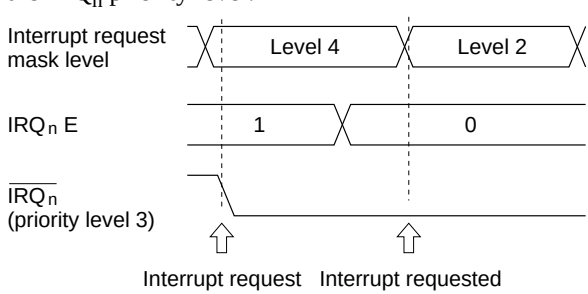
Classification—H8/500

	Registers
	Read timing
	Write timing
❍	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. When an IRQ_n interrupt request is held pending because of the interrupt request mask level (I_2 to I_0), the request remains pending even if IRQ_nE is cleared to 0.

   The IRQ_n interrupt will be accepted later when the interrupt request mask level is reduced to a value less than the IRQ_n priority level.



Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

IRQ_0 is level-sensitive, so it is not held pending, regardless of whether IRQ_0E is set or cleared.

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 035A
Topic	Acceptance of NMI during NMI handling		

Question

1. NMI has the highest priority and is always accepted. During the NMI interrupt handling routine, if another NMI interrupt occurs will it also be accepted?

Classification—H8/500

	Registers
	Read timing
	Write timing
❍	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. If another NMI request is made during the NMI interrupt handling routine, the second request will also be accepted.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 009B – 1
Topic	NMI sampling and acceptance immediately after a reset		

Question

1. When is the $\overline{\text{NMI}}$ signal first sampled after a reset?

	Classification—H8/500
	Registers
	Read timing
	Write timing
	Interrupts
❍	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. Sampling of the $\overline{\text{NMI}}$ signal starts from the first falling edge of the system clock at which the reset signal is high. The NMI interrupt becomes acceptable when the first instruction has been executed after the chip comes out of reset.

(See next page)

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

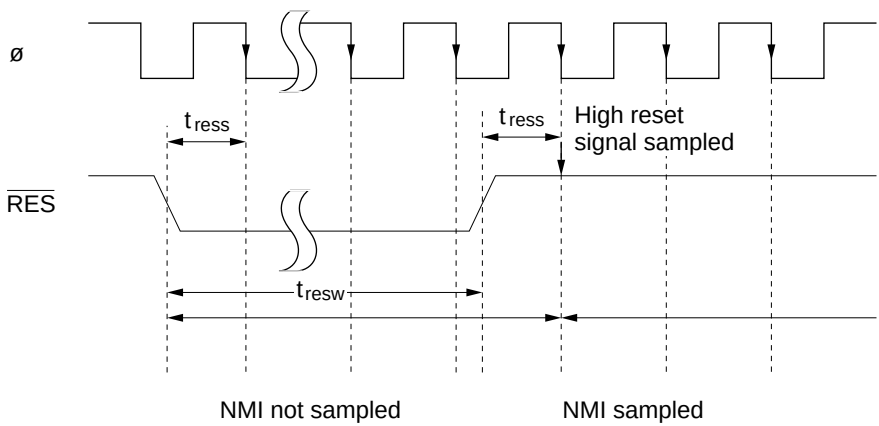
Additional Information

The reset and NMI signals are both sampled on the falling edge of the system clock.

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 009B – 2
Topic	NMI sampling and acceptance immediately after a reset		
Question			

[Example]



Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 010B
Topic	Stack pointer initialization immediately after a reset		

Question

1. Why is it necessary to initialize the stack pointer immediately after a reset?

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
❍	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. If the $\overline{\text{NMI}}$ request signal is active when the chip comes out of reset, the NMI interrupt will be accepted as soon as the first instruction has been executed. To prevent program crashes, you should therefore initialize the stack pointer immediately after the reset.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 037A
Topic	Pin states at power-up reset		

Question

1. What needs to be noted about pin states at a power-up reset?

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
❍	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. At a power-up reset, the mode pins (MD_2 to MD_0) must be tied to the desired mode setting and the $\overline{STBY}$ pin must be held high. Output from the ø and E pins is unpredictable until the clock oscillator settles into steady oscillation.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

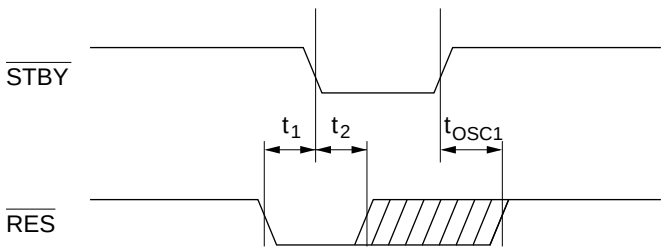
When using a microcontroller that multiplexes the ø and E pins with general-purpose input ports, connect a resistor with a resistance of several kilohms in series with these pins.

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 011B
Topic	Hardware standby mode entry timing		

Question

1. Are there any restrictions on times t_1 and t_2 in the diagram below for entering hardware standby mode?

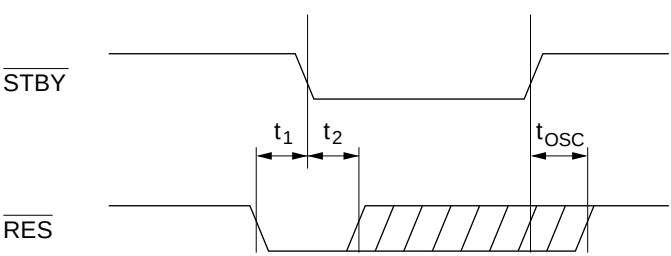


Answer

1. The following restrictions apply.

   (1) To hold RAM contents, t_1 must be at least 10 system clock cycles. The minimum value of t_2 is 0 ns.

   (2) When it is not necessary to hold RAM contents, there is no restriction on t_1 and t_2.



Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
❍	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 013B
Topic	Instruction execution at changeover to hardware standby mode		

Question

1. When a low $\overline{\text{STBY}}$ input drives the chip into hardware standby mode, what happens to the instruction currently being executed?

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
❍	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. The instruction being executed is aborted, without being completed. Normal execution of the instruction is not assured.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 014B
Topic	Mode pins in hardware standby mode		

Question

1. What happens if the states of the mode lines (MD_2 to MD_0) are changed during hardware standby mode?

Answer

1. Hardware standby mode will not operate correctly. Do not change the state of the mode lines during hardware standby mode.

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
❍	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 016B
Topic	Recovery from hardware standby mode		

Question

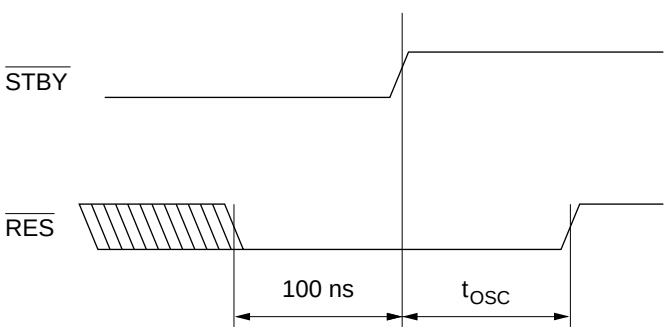
1. The chip must be recovered from hardware standby mode by holding $\overline{\text{RES}}$ low, then driving $\overline{\text{STBY}}$ high. How long before $\overline{\text{STBY}}$ goes high does $\overline{\text{RES}}$ have to go low?

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
❍	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. To recover from hardware standby mode, drive $\overline{\text{RES}}$ low at least 100 ns before driving $\overline{\text{STBY}}$ high.



Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 019B
Topic	Notes on entering sleep mode		

Question

1. Are there any points to note about entering sleep mode?

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
❍	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. The points listed below should be noted, depending on the method used to recover from sleep mode.

Recovery Method

NMI Interrupt	IRQ_n Interrupt
Clear all interrupt enable bits to 0, or set bits I_2 to I_0 in SR all to 1.	Set bits I_2 to I_0 in SR to a level lower than the priority level of the interrupt used for recovery, clear interrupt enable bits to 0 except for interrupts used for recovery, and make sure NMI is not requested.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 020B
Topic	Interrupts during fetching and execution of SLEEP instruction		

Question

1. What happens if an interrupt is accepted while the SLEEP instruction is being executed?

Answer

1. Sleep mode is released to handle the interrupt. At the end of interrupt handling, the next instruction after the SLEEP instruction is executed.

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
❍	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 021B
Topic	Sampling and acceptance of interrupts during sleep mode		

Question

1. When are external interrupts sampled during sleep mode?

2. If an interrupt is sampled, how many system clock cycles later does the chip wake up?

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
❍	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. Level-sensitive interrupts (IRQ_0) are sampled on the rising edge of the system clock and edge-sensitive interrupts (external interrupts other than IRQ_0) are sampled on the falling edge of the system clock, just as in active mode.

2. The chip exits sleep mode six system clock cycles after the interrupt is sampled.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 027A
Topic	Execution time for entering software standby mode		

Question

1. How many states does it take to enter software standby mode by executing the SLEEP instruction?

Answer

1. Two states.

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
❍	Power-down state
	Instructions
	Software
	Development tools
	Miscellaneous

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 023B
Topic	BRN instruction		

Question

1. What sort of instruction is BRN (or BF)?

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
	Power-down state
❍	Instructions
	Software
	Development tools
	Miscellaneous

Answer

1. BRN is similar to a NOP instruction, but it has a different byte length and executes in a different number of states. See below.

		Byte Length	Number of States Required for Execution
BRN	d: 8	2	3*
	d: 16	3	3*
NOP		1	2*

* When instruction is fetched from on-chip ROM

BRN has the same byte length as Bcc, for example, which makes it useful in debugging.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 033A
Topic	Reserved addresses in interrupt vector area		

Question

1. Can the reserved addresses in the interrupt vector area be used to store program code?

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
❍	Software
	Development tools
	Miscellaneous

Answer

1. Yes, they can.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500 CPU	Q&A No.	QA8500 - 029A
Topic	Access to on-chip registers while bus is released		

Question

1. When the H8/500 CPU releases the bus to an external device, can the external device (bus master) access the H8/500's on-chip registers?

Classification—H8/500

	Registers
	Read timing
	Write timing
	Interrupts
	Reset
	External expansion
	Power-down state
	Instructions
	Software
	Development tools
❍	Miscellaneous

Answer

1. No. On-chip registers cannot be accessed externally under any circumstances.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information